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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,026	06/23/2003	Jeffrey P. Gambino	FIS920030130US1	1025

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/604,026	GAMBINO ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *20-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-19 in Paper No. 3 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

3. Claims 1, 2, 4-9, 11-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin (US Pat. Application Pub. 2004/0108217) in view of Omura (US Pat. 6028362).

Regarding claims 1 and 6, Dubin discloses an interconnect structure/IS (Fig. 3) formed on a substrate (102 in Fig. 3), the structure comprising:

- a first layer of a first dielectric material having a first conductor embedded therein (104 and 112 respectively in Fig. 3), the first conductor having a top surface coplanar with a top surface of the first layer of the dielectric material

- a second layer of a second dielectric material overlying the first layer of dielectric material and having a second conductor embedded therein (104' and 112' respectively in Fig. 3)
- the second conductor comprising at least a first portion and a second portion wherein the first portion is in electrical contact with the first conductor, the second portion overlying and in electrical contact with the first portion (see damascene structure in Fig. 3), the second portion having a lateral dimension/extent greater than that of the first portion, and
- the second portion having a top surface coplanar with a top surface of the second layer of dielectric material (see Fig. 3)

(Fig. 3; section 0029; Fig. 1-3; sections 0015-0031).

Dubin fails to teach the second portion of the second conductor being formed of a different material than that of the first portion.

Omura teaches a dual-damascene interconnect structure/DIS (Fig. 4-11) having a conductor (52S/44S in Fig. 11), the conductor comprising first and second portions where the second portion has a lateral dimension/extent greater than that of the first portion (see holes 44S and 46S/52S respectively in Fig. 4-11; Col. 8) and the second portion and the first portion are formed of different material such as copper (Col. 11, line 29-Col. 12, line 26) and tungsten (Col. 9, lines 33-66) respectively to achieve an

improved surface coverage and reliability, reduced void formation and the desired wiring resistance (Col. 9, line 33- Col. 12, line 65; Col. 19, lines 16-43).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second portion of the second conductor being formed of a different material than that of the first portion as taught by Omura so that the void formation can be reduced and the conductor filling/coverage and reliability can be improved in Dubin's IS.

Regarding claims 2 and 7, Dubin and Omura teach substantially the entire structure as applied to claim 1 above, wherein Dubin teaches using a barrier/conductive liner being disposed in the first and second portions (108/108' in Fig. 3), the barrier/conductive liner being formed of a conventional material such as titanium, tantalum, etc. (section 0021), but fail to teach:

- a first conductive liner disposed between the first portion and the second dielectric material and between the first portion and the first conductor and a second conductive liner disposed between the second portion and the second dielectric material and between the second portion and the first portion, and
- and the second liner being formed of a material different from that of the first liner.

Omura further teach the DIS having first and second barrier layers/conductive liners/adhesion layers in the first and second portions of the conductor respectively (see 50S and 50S/54S in Fig. 11, 27A/27B, etc.) where the first conductive liner disposed between the first portion and the second dielectric material and between the first portion and the first conductor (see 50S in Fig. 27A/27B) and a second conductive liner disposed between the second portion and the second dielectric material and between the second portion and the first portion (see 50S/54S in Fig. 27A/27B). Furthermore, the barrier layers/conductive liners/adhesion layers 50S and 54S are formed of a variety of material including titanium (Ti), titanium nitride (TiN), titanium-tungsten (TiW), etc. (see material for the layer 50S: Col. 9, lines 1-26) and TiN, TiW, TiON, a lamination of metal silicide/nitride, etc. (see material for the layer 54S: Col. 10, lines 41-56) to achieve the desired conformality and adhesion/barrier properties (Col. 9-11; Col. 18 and 19).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first conductive liner disposed between the first portion and the second dielectric material and between the first portion and the first conductor and a second conductive liner disposed between the second portion and the second dielectric material and between the second portion and the first portion where the second liner is formed of a material different from that of the first liner as taught by Omura so that the desired adhesion/barrier properties can be achieved, the surface coverage/uniformity can be improved and the back-end processing can be simplified in Omura and Dubin's IS.

Regarding claims 4 and 5, Dubin and Omura teach substantially the entire structure as applied to claim 1 above, wherein Dubin further teaches the first and second dielectric layers being formed from a variety of material and having layers or laminations with different thickness including silicon oxide, organic or inorganic dielectric, etc. to provide the desired insulation/dielectric properties (sections 0018 and 0019).

Regarding claim 8, Dubin and Omura teach substantially the entire structure as applied to claim 1 above, except the second liner having a thickness being less than that of the first liner.

Omura further teaches the barrier layers/conductive liners/adhesion layers 50S and 54S being formed of a variety of material including titanium (Ti), titanium nitride (TiN), titanium-tungsten (TiW), etc. (see material for the layer 50S: Col. 9, lines 1-26) and TiN, TiW, a lamination of refractory metal/nitride, TiON, etc. (see material for the layer 54S: Col. 10, lines 41-56) to achieve the desired conformality and adhesion/barrier properties (Col. 9-11; Col. 18 and 19). Furthermore, the thickness of such layers can range from 57nm (see the thickness of 50S: Col. 10, lines 40-50) to 55-250nm (see the thickness of 54S: Col. 9, lines 1-10).

The determination of parameters such as thickness of barrier layers/liners, number of such layers, spacing, etc. thickness/type of wiring layer, etc. in chip packaging and multilevel interconnect (MLI) technology is a subject of routine

experimentation and optimization to achieve the desired dielectric properties, electrical performance, resistance, conformality/surface coverage, pinhole/void formation, etc.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second liner having a thickness being less than that of the first liner as taught by Omura so that the desired electrical properties including the desired effect/contribution on the overall resistance due to the thickness can be achieved and the back-end processing can be simplified in Omura and Dubin's IS.

Regarding claims 9 and 13, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2 and 8 above.

Regarding claims 11 and 12, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2, 8, 9, 4 and 5 above.

Regarding claim 14, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2, 8, 9 and 7 above.

Regarding claim 15, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2, 8 and 9 above, wherein Dubin teaches another conductive

barrier/liner being disposed on the first barrier layer/liner (see 110 in Fig. 1e; section 0022).

Regarding claims 17 and 18, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2, 8, 9, 15, 4 and 5 above.

Regarding claim 19, Dubin and Omura teach substantially the entire structure as applied to claims 1, 2, 8, 9, 15 and 7 above.

4. Claims 3, 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin (US Pat. Application Pub. 2004/0108217) and Omura (US Pat. 6028362) as applied to claims 1 and 9 above, and further in view of Jain (US Pat. 5821168).

Regarding claims 3, 10 and 16, Dubin and Omura teach substantially the entire structure as applied to claims 1, 9 and 15 above, except a hardmask layer overlying the second layer of dielectric material wherein the second portion of the second conductor has a top surface being coplanar with a top surface of the hardmask layer.

Jain teaches a DIS where a barrier/hardmask layer is formed above a dielectric /second dielectric layer (see 56 and 54 respectively in Fig. 9) such that a second portion of a conductor/second conductor has a top surface coplanar with the top surface of the barrier/hardmask layer (see Fig. 9; Col. 3, line 25- Col. 5, line 53).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the hardmask layer overlying the second layer of dielectric material wherein the second portion of the second conductor has a top surface being coplanar with the top surface of the hardmask layer as taught by Jain so that the planarization/etch back and the top surface planarity/uniformity can be improved in Omura and Dubin's IS.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

06-25-04

PATENT EXAMINER

TECHNOLOGY CENTER 2800